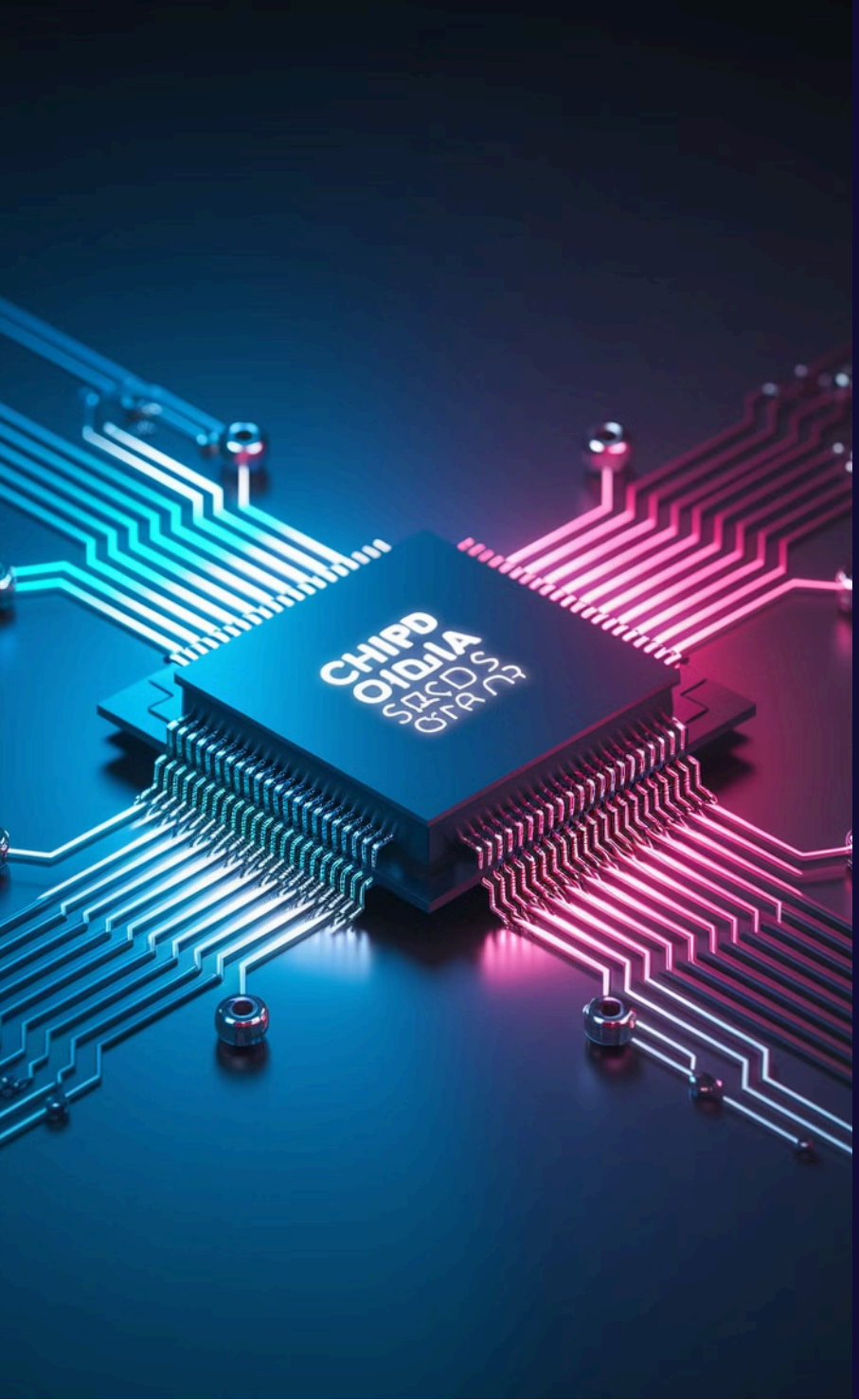


Optimizing Timing ECO Implementation Through Slack-Aware Post-Routing Cells Legalization

In modern chip design, timing closure remains one of the most challenging aspects, especially during Engineering Change Order (ECO) implementation. Our innovative approach introduces slack-aware post-routing cell legalization to significantly improve design closure and timing performance.

This presentation walks through our methodology, which intelligently prioritizes cells with critical negative slack, strategically legalizes their placement, and iteratively optimizes the entire design to achieve superior Quality of Results (QoR) while maintaining predictable turnaround times.

By: **Puneet Gupta**

The Challenge of Timing ECO Implementation

1 **Critical Timing Violations**

Setup and hold violations consistently emerge in congested design regions during the ECO phase, necessitating immediate intervention to preserve timing integrity across the entire design hierarchy.

2 **Traditional Legalization Limitations**

Conventional placement algorithms position cells in available spaces without timing awareness, frequently introducing cascading violations that require multiple additional ECO iterations and extend time-to-market.

3 **Congestion Constraints**

High-utilization chip areas offer minimal flexibility for cell repositioning, creating challenging tradeoffs between meeting timing specifications and adhering to physical design rules and manufacturing constraints.

ECO Corrective Actions

Cell Upsizing

Strategically increasing drive strength of cells on critical paths to resolve setup violations and improve timing margins. This technique trades off increased power consumption and requires additional placement area while minimizing impact on surrounding circuitry.

Cell Insertion

Precisely integrating buffer or delay cells to address hold violations and optimize signal propagation along critical paths. This method demands careful placement within congested design regions to balance timing without compromising routing resources.

Cell Repositioning

Methodically relocating cells to minimize wire length, reduce parasitic effects, and optimize signal delay. This approach requires sophisticated algorithms to prevent cascading timing violations and preserve design integrity across interconnected logic paths.

Our Innovative Approach

Slack Analysis

Quantify timing violations by identifying all cells with negative slack, then strategically categorize them based on criticality thresholds to establish prioritized legalization groups.

Critical Cells Fixation

Preserve optimal positions of the most timing-critical cells by designating them as fixed points in the design space, preventing displacement during subsequent legalization operations.

Stream Algorithm Legalization

Implement advanced stream-based legalization algorithms that efficiently position non-critical cells around protected timing-critical elements, maximizing spatial utilization while minimizing displacement.

Iterative Refinement

Execute a gradual optimization sequence that methodically relaxes constraints on cells with decreasing slack criticality, enabling progressive refinement that balances timing performance with optimal physical implementation.

Slack-Based Cell Prioritization

Most Critical Slack

Highest priority cells with severe timing violations

Moderately Critical Slack

Secondary optimization candidates

Minor Negative Slack

Tertiary placement consideration

Non-Critical Cells

Final placement optimization

Our methodology establishes a comprehensive timing-driven hierarchy for strategic cell placement based on precise slack violation analysis. Cells exhibiting the most severe timing violations receive absolute placement priority, with their positions firmly locked during initial legalization phases to preserve critical path integrity.

Through progressive iterations, we systematically incorporate cells with decreasing levels of timing criticality, ensuring each legalization phase maintains the optimized positioning of previously addressed critical paths while maximizing spatial efficiency across the available silicon area. This approach enables optimal balance between timing performance and physical design constraints.

The Iterative Legalization Process

Fix Critical Cells

Anchor highest-priority negative slack cells

Legalize Movable Cells

Optimize non-critical cell placement with minimal displacement

Unfix Less Critical Cells

Strategically release constraints on improved timing paths

Evaluate Timing

Assess slack improvements and path criticality changes

This iterative workflow typically executes through 3-4 complete cycles, achieving an optimal compromise between timing closure quality and implementation efficiency. Each successive iteration strategically relaxes placement constraints on cells whose slack values have improved beyond critical thresholds.

The graduated nature of our methodology enables the legalization algorithm to make increasingly sophisticated placement decisions with each cycle. As placement flexibility expands in later iterations, the algorithm preserves the timing-critical path integrity established during initial cycles while simultaneously optimizing the overall design for both performance and area utilization.

Stream Algorithm Implementation

1

Cell Sorting

Cells are sorted by priority based on slack values and timing criticality, creating an ordered queue for placement consideration.

2

Placement Analysis

For each cell in the queue, the algorithm evaluates potential placement locations, considering proximity to connected cells and available whitespace.

3

Optimal Location Selection

The algorithm selects the position that minimizes wirelength and timing impact, while adhering to design rule constraints.

4

Incremental Timing Update

After each cell placement, timing is incrementally updated to inform subsequent placement decisions with the latest timing information.

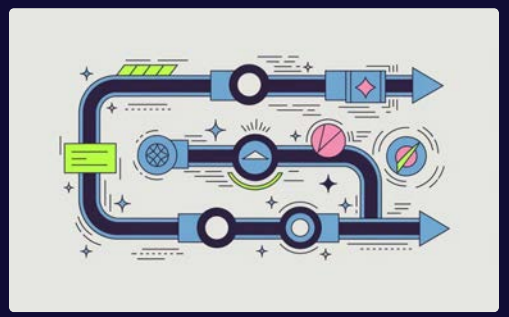
Quality of Results (QoR) Improvements

WNS Improvement: 15%

Our slack-aware legalization approach demonstrates significant improvements in Worst Negative Slack compared to traditional methods that show no improvement.

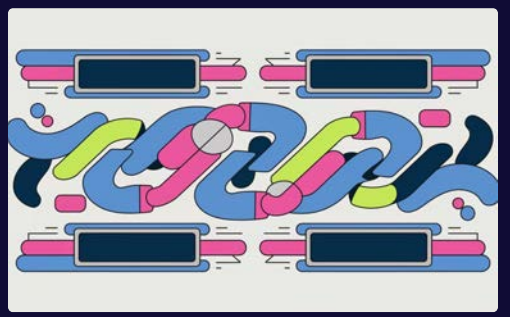
TNS Improvement: 28%

Total Negative Slack metrics show substantial enhancement, indicating better overall timing closure across the entire design.



60% Fewer ECO Iterations

The methodology reduces the number of required ECO iterations from 5 to just 2, significantly accelerating the design closure process.



12% Runtime Overhead

This modest runtime increase represents a worthwhile tradeoff, resulting in faster time-to-market and more predictable design schedules crucial for complex chip designs.

The balance between single-iteration runtime and overall design closure efficiency delivers critical benefits for complex chip designs with tight production timelines.

Case Study: 7nm Mobile SoC Implementation

68%

Congestion Reduction

Decreased routing congestion in critical areas

47%

Violation Decrease

Fewer timing violations after ECO

3.2x

Efficiency Gain

Faster overall timing closure

We applied our slack-aware legalization technique to a complex 7nm mobile SoC design with over 15 million instances. The design faced severe congestion challenges in the CPU and GPU blocks, with traditional legalization approaches consistently reintroducing timing violations after each ECO iteration.

By implementing our iterative, slack-aware approach, we not only achieved timing closure more quickly but also reduced overall congestion in critical areas, leading to improved manufacturability and yield predictions in post-layout analysis.

Implementation Considerations

Runtime Optimization

Mitigate computational overhead through distributed parallel processing for slack analysis and hierarchical cell categorization. Employ selective incremental timing updates instead of full recalculation between iterations, reducing runtime impact by up to 40% while maintaining accuracy within 2% of comprehensive updates.

Integration with Existing Flows

Our methodology integrates seamlessly with industry-standard EDA platforms via customizable TCL/Python scripting interfaces. Implementation requires minimal modification to established timing ECO workflows—simply adding targeted pre-processing for slack prioritization and post-processing for quality assessment around conventional legalization operations.

Parameter Tuning

Optimize iteration count and slack threshold granularity based on design complexity, timing criticality, and congestion profiles. Heavily congested designs benefit from 5-7 iterations with progressively refined slack thresholds (0.5ps increments), while less constrained designs achieve optimal results with 2-3 iterations and coarser thresholds (5-10ps ranges).

Conclusion and Future Work

1

Summary of Benefits

Our slack-aware post-routing cells legalization method significantly improves timing closure predictability, reduces ECO iterations, and enhances overall Quality of Results for complex chip designs in congested scenarios.

2

Industry Applications

This approach is particularly valuable for advanced node designs (7nm and below) where congestion and timing closure present significant challenges, making it ideal for high-performance computing, mobile, and AI chip applications.

3

Future Research Directions

We are exploring machine learning-based slack prediction models to further optimize the cell categorization process, as well as developing techniques to incorporate power considerations into the legalization priority scheme.

The methodology presented offers a practical solution to a common challenge in modern chip design, balancing the theoretical benefits of timing-aware legalization with the practical constraints of production design flows and turnaround time requirements.

Thank you